2. The method of Claim 1, further comprising the steps of:

(E) shifting the second plurality of bits, wherein the second plurality of bits has a second value; and

(F) loading the least significant bit with the next bit.

3. The method of Claim 1, wherein step (C) comprises generating the next bit in the serial pattern having the same state as the least significant bit in the second plurality of bits if the first value is not equal to the at least one number, and wherein step (D) comprises generating the next bit in the serial pattern having the complement state as the least significant bit in the second plurality of bits if the first value is equal to the at least one number.

4. The method of Claim 1, wherein the second plurality of bits comprises n bits, and the at least one number comprises one through 2^{n-1} inclusive.

5. The method of Claim 1, wherein the second plurality of bits comprises n bits, and the at least one number comprises $2^{n-1} - 1$ through $2^{n} - 2$ inclusive.

6. A pattern generator comprising:

a sequence generator outputting a serial sequence of bits and a plurality of bits having a value;

a comparator coupled to the sequence generator, the comparator receiving the plurality of bits and at least one number, wherein the comparator compares the value with the at least one number and generates a comparison result; and

a next bit generator coupled to the comparator and the sequence generator, wherein the next bit generator receives the comparison result and one of the plurality of bits, and wherein the next bit generator generates a next bit for the serial sequence of bits.

7. The pattern generator of Claim 6, wherein the comparison result is a first result value when the value of the plurality of bits is equal to the at least one number, and wherein the comparison result is a second result value when the value of the plurality of bits is not equal to the at least one number.

8. The pattern generator of Claim 7, wherein the next bit is a same state as the one of the plurality of bits if the comparison result is the first result value, and wherein the next bit is a complement state of the one of the plurality of bits if the comparison result is the second result value.

9. The pattern generator of Claim 7, wherein the next bit is a same state as the one of the plurality of bits if the comparison result is the second result value, and wherein the next bit is a complement state of the one of the plurality of bits if the comparison result is the first result value.

10. The pattern generator of Claim 6, further comprising:

a memory coupled to the comparator, wherein the memory stores the at least one number.

11. The pattern generator of Claim 6, wherein the next bit generator comprises an exclusive OR (XOR) logic gate.

12. The pattern generator of Claim 6, wherein the sequence generator comprises a plurality of registers, wherein the plurality of registers are coupled to one another such that they receive the next bit from the next bit generator and output the plurality of bits to the comparator.

13. The pattern generator of Claim 6, wherein the plurality of bits comprises n bits, and the at least one number comprises one through 2^{n-1} inclusive.

14. The pattern generator of Claim 6, wherein the plurality of bits comprises n bits, and the at least one number comprises $2^{n-1} - 1$ through $2^{n} - 2$ inclusive.

15. The pattern generator of Claim 6, wherein the pattern generator is included in a system, the system further comprising:

a device under test coupled to the pattern generator and receiving the serial sequence of bits, wherein the device under test is tested in response to the serial sequence of bits.

16. The pattern generator of Claim 15, wherein the device under test comprises a memory device, a programmable logic device, a data communications device, a built-in self-test circuit (BIST), or a digital signal processing device.

17. A medium readable by a digital signal processing device, the medium storing a sequence of instructions for generating a pattern comprising a first plurality of bits, wherein the sequence of instructions causes the digital signal processing device to:

(A) generate a second plurality of bits having a first value and a least significant bit, wherein the second plurality of bits includes less bits than the first plurality of bits;

(B) compare the first value with at least one number;

(C) if the first value is equal to the at least one number, then generate a next bit in the pattern having a same state as the least significant bit in the second plurality of bits; and

(D) if the first value is not equal to the at least one number, then generate the next bit in the pattern having a complement state of the least significant bit in the second plurality of bits.

18. The medium of Claim 17, wherein the sequence of instructions further causes the digital signal processing device to:

(E) shift the second plurality of bits, wherein the second plurality of bits have a second value; and

(F) load the least significant bit with the next bit.